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Customer No.: 23,569

PATENT

NBD-48/47181-00259

APPLICATION FOR UNITED STATES LETTERS PATENT

for

ARC FAULT CIRCUIT INTERRUPTER SYSTEM

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EXPRESS MAIL MAILING LABEL

NUMBER EJ544175083US

DATE OF DEPOSIT 10/17/2001

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ARC FAULT CIRCUIT INTERRUPTER SYSTEM

FIELD OF THE INVENTION

The present invention relates to the protection of electrical circuits and, more particularly, to the detection of electrical faults of the type known as arcing faults in an electrical circuit.

BACKGROUND OF THE INVENTION

The electrical systems in residential, commercial and industrial applications usually include a panelboard for receiving electrical power from a utility source. The power is then routed through protection devices to designated branch circuits supplying one or more loads. These overcurrent devices are typically circuit interrupters such as circuit breakers and fuses which are designed to interrupt the electrical current if the limits of the conductors supplying the loads are surpassed.

Circuit breakers are a preferred type of circuit interrupter because a resetting mechanism allows their reuse. Typically, circuit breakers interrupt an electric circuit due to a disconnect or trip condition such as a current overload or ground fault. The current overload condition results when a current exceeds the continuous rating of the breaker for a time interval determined by the trip current. A ground fault trip condition is created by an imbalance of currents flowing between a line conductor and a neutral conductor which could be caused by a leakage current or an arcing fault to ground.

Arcing faults are commonly defined as current through ionized gas between two ends of a broken conductor or at a faulty contact or connector, between two conductors supplying a load, or between a conductor and ground. However, arcing faults may not cause a conventional circuit breaker to trip. Arcing fault current levels may be reduced by branch or load impedance to a level below the trip curve settings of the circuit breaker. In addition, an arcing fault which does not contact a grounded conductor or person will not trip a ground fault protector.

There are many conditions that may cause an arcing fault. For example, corroded, worn or aged wiring, connectors, contacts or insulation, loose connections, wiring damaged by nails or staples through the insulation, and electrical stress caused by

repeated overloading, lightning strikes, etc. These faults may damage the conductor insulation and/or cause the conductor to reach an unacceptable temperature.

OBJECTS AND SUMMARY OF THE INVENTION

It is an object of the present invention to provide an arc fault detection system and method which reliably detects arc fault conditions which may be ignored by conventional circuit interrupters.

Another object of the invention is to provide an arc fault detection system which utilizes a minimum number of highly reliable electronic signal processing components, such as a microcontroller, to perform most of the signal processing and analyzing functions, so as to be relatively simple and yet highly reliable in operation.

Other and further objects and advantages of the invention will be apparent to those skilled in the art from the present specification taken with the accompanying drawings and appended claims.

In accordance with one aspect of the invention, there is provided a system for determining whether arcing is present in an electrical circuit in response to a sensor signal corresponding to current in said circuit, said system comprising a circuit for analyzing said sensor signal to determine the presence of broadband noise in a predetermined range of frequencies, and producing a corresponding output signal, and a controller for processing said sensor signal and said output signal to determine current peaks and rise times and to determine, using said current peaks and rise times and the presence of broadband noise, whether an arcing fault is present in said circuit, by comparing data corresponding to said current peaks and rise times and broadband noise with preselected data indicative of an arcing fault, wherein said circuit for analyzing and said controller are integrated onto a single application specific integrated circuit chip.

In accordance with another aspect of the invention, there is provided a method for determining whether arcing is present in an electrical circuit in response to a sensor signal corresponding to current in said circuit, said method comprising, on a single application specific integrated circuit chip analyzing said sensor signal to determine the presence of broadband noise in a predetermined range of frequencies, and producing a corresponding output signal, and processing said sensor signal and said output signal to determine current peaks and rise times and to determine, using said current peaks and rise times and

the presence of broadband noise, whether an arcing fault is present in said circuit, by comparing data corresponding to said current peaks and rise times and broadband noise with preselected data indicative of an arcing fault.

In accordance with another aspect of the invention, there is provided a system for determining whether arcing is present in an electrical circuit in response to a sensor signal corresponding to current in said circuit, said system comprising, on a single application specific integrated circuit chip, means for analyzing said sensor signal to determine the presence of broadband noise in a predetermined range of frequencies, and producing a corresponding output signal, and means for processing said sensor signal and said output signal to determine current peaks and rise times and to determine, using said current peaks and rise times and the presence of broadband noise, whether an arcing fault is present in said circuit, by comparing data corresponding to said current peaks and broadband noise with preselected data indicative of an arcing fault;

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

FIG. 1a and 1b form a circuit schematic of an arc fault circuit interrupter system in accordance with the invention;

FIG. 2 is a functional diagram showing further details of an application specific integrated circuit chip which forms a part of a system of FIG. 1;

FIG. 3 is a functional block diagram illustrating operation of a digital circuit portion of the chip of FIG. 2; and

FIG. 4 is a circuit schematic of a signal processing circuit which forms a part of the chip of FIG. 1b.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENT

This invention pertains to the use of a system on chip solution for arc fault detection primarily for use in circuit breakers or electrical outlet receptacles, or other electrical devices, typically but not limited to the 15 or 20 ampere size. Referring to FIGS. 1a and 1b, this microchip 10, when incorporated on an electronic printed wiring board 12 with a minimum of external components, provides arc fault detection and tripping of the host wiring device.

The system on chip is an application specific integrated circuit which combines analog and digital signal processing on a single microchip. A block diagram is shown in FIG. 2.

The "system on chip" 10 monitors line voltage and current in the host device and analyzes them for the presence of an arc fault. If certain arc detection criteria are met as determined by an arcing algorithm embedded within the software of a microcontroller's 10 memory 18, the chip signals an external SCR98 causing it to disconnect the device from the load.

The ASIC generally includes a processor or microcontroller 14, memories, amplifier stages, filters, A/D converter, analog multiplexer, a voltage regulator and power on reset circuit. The tasks of the ASIC are: measure line voltage, detect voltage zero crossings, measure 60 Hz line current, measure ground fault current, detect ground loops (grounded neutral) in neutral line, detect high frequency components of line current, provide voltage regulation for all ASIC circuits, detect presence of a signal to commence self test, generate a self test high frequency current source, provide undervoltage reset (POR) for the microcontroller, provide a trip signal to fire a trip solenoid driver, provide a watchdog to reset the microcontroller, and make a trip decision based on embedded code in the microcontroller.

The ASIC can operate in two different modes:

The "normal" mode corresponds to the mode where the processor 14 is the master. In normal mode, the microprocessor controls the data conversion rate (A-to-D), counters, interruptions and data memories. The microprocessor executes code stored in a ROM memory. Moreover, the microprocessor controls the activity of all analog blocks by forcing "power down" signal in order to limit the power dissipation. This mode is the normal operation mode of the ASIC.

The "slave" mode corresponds to the mode where the processor 14 is the slave and is controlled by a standard communication channel (e.g., a JTAG) interface or port 15 (see FIGS. 1a and 1b). Two main operations can be done in this mode using the JTAG interface 15: debug mode, and register values and data transfer. The JTAG port can be used to couple a personal computer (PC) or other external processor to the ASIC, using the processor 14 of the ASIC as a slave processor. This permits interrogation of the ASIC counters, registers, etc. as well as rewriting to memories, registers, etc. of the

ASIC. The JTAG ports 15 include data in/out ports (TDI, TDO), and reset (TRST), clock (TCLK) and mode select (TMS) ports.

The processor 14, in one embodiment, is the ARM7TDMI from ARM company. The ARM has a boundary scan circuit around its interface which is used for production test or for connection to an in-circuit emulator (ICE) interface (i.e., the JTAG) for system and software debugging. The JTAG interface is accessible via the pins TDI, TDO, TMS, TCK and TRST and behaves as specified in the JTAG specification.

The processor is 32 bit wide and has a CPU frequency of 4 MHz. An external resonator 90 (FIG. 1b) has a frequency of 8 MHz which is divided by two for the CPU. The microprocessor analyzes the current, ground fault and di/dt signals and by means of an arc detection algorithm makes a trip decision, using the presence of broadband noise and the current peaks and rise time (di/dt). One such algorithm is described in U.S. Patent No. 6,259,996, issued July 10, 2001 to which reference is invited. While the line voltage is fed to the microprocessor, it may be optionally used by the algorithm to effect various levels of arc detection as dictated by the embedded software. The microprocessor uses the zero crossing signal to synchronize the arc detection algorithm with line voltage. There are different clock domains in the ASIC: A clock for the ARM, the bus controller and the memories. The microprocessor clock frequency is 4 MHz. Clocks for the peripherals (counters, watchdog, ADC, BP filters) are 4 MHz, 1 MHz and 250 KHz frequencies. These clocks are fixed and derived from the ARM clocks.

There are two memory domains. The program memory, which contains the software for the ARM operation, the program memory space contains a 10 kb ROM (2560 words of 32 bits), and the program memory start address is 0000:0000hex. The data memory 16 contains the program data and consists of two RAMs of 128 bytes x 16 bits for a total of 512 bytes. The memory access can be 32 bits or 16 bits wide. The ARM selects the access mode. The data memory start address is 0004:0000hex. In addition to the memories, the processor can also access registers. The register memory start address is 0008:0000hex.

The various functional blocks (see FIG. 2) and their respective operation is described briefly below:

A 3.3V regulator 20 provides a finely regulated DC power source for use by the analog and digital sections of the chip. The input to the chip need only be roughly regulated to within coarse limits, for example 4 to 7 volts.

The POR or power on reset circuit 22 senses the chip's regulated voltage supply and holds the microcontroller in a reset state if the voltage is below a safe operating limit.

The analog reference circuit (AREF) 24 provides a reference point for the input signals at the midpoint of the analog power supply to allow the amplified signals to swing both positive and negative. The AREF is externally connected to the REFIN pin 26.

A Vl/Vn differential amplifier 28 differentially measures line voltage at the terminals of the host device via an externally located voltage divider 29 (FIG. 1b). The voltage signal is low pass filtered as shown at the low pass filter block 30 to remove high frequency noise or harmonics and to provide anti-aliasing. The filtered signal is sent to a first channel of a multiplexer 32 and also to the input of a zero crossing detector 34. The output voltage at VCAP pin and an external capacitor 91 (FIG. 1b) provides an anti-aliasing low-pass filter (LPF) for the A/D converter 86. The typical differential input range at the inputs is +/-0.65V.

A comparator 34 at the output of the line voltage differential amplifier 28 detects zero crossings (ZC) in the line voltage for use in synchronizing an arc detection algorithm.

An amplifier 36 at the INTEG input amplifies the externally integrated output of a di/dt sensor before it is lowpass filtered 38 for anti-aliasing and sent to a second channel of the multiplexer 32 previously referenced.

The output of a di/dt sensor 25 (see FIG. 1) monitoring line current through the host device is connected to the input of a di/dt amplifier 40 after first being high pass filtered by filter capacitors 42 (FIG. 1b) to remove the 60 Hz component. The di/dt signal is amplified at amplifier 40 and sent to the input of three bandpass filters 50, 52, 54. Broadband noise in the 10 KHz to 100 KHz range appearing at the DIDT input is one indicator of the presence of arcing.

FIG. 3 shows a more detailed block diagram of the di/dt sensing system. Three switched cap (SC) bandpass filters (BPF) 50, 52, 54 set respectively at 20, 33 and 58 KHz, filter the di/dt signal to determine if there is broadband noise in the line current. The 20 KHz filter 50 is provided for added flexibility in future arc detection devices. The output of the filters is monitored by a set of comparators 60 whose outputs change state

when a predetermined threshold is exceeded. The microprocessor 14 (FIG. 2) monitors the state of each filter's comparator individually and also the logically ANDed output at AND gates 62 of the 33 and 58 KHz filters to determine the presence of broadband noise. The comparator 60 outputs and the AND gates 62 are synchronized by the same clock (f = 1 MHz) as the switched capacitor bandpass filters 50, 52 54. It should be noted that the ANDing of the comparator outputs with the clock insures that the components of high frequency in the passbands of both the 33 KHz and 58 KHz filters must be simultaneously present and of sufficient amplitude in order to be considered broadband noise and therefore be counted by the 33/58 counter. Separate counters are provided for future use, for counting the components in the passbands of the 20 KHz, 33 KHz and 58 KHz BPF's, respectively.

The ASIC provides an amplification of the di/dt input signal and performs analog signal processing. As described above, the signal going through three independent switched-cap bandpass filters (BP) (20, 33 and 58 KHz) is compared to a fixed threshold reference voltage in both directions (positive and negative). The 20 KHz BP has a typical quality factor Q of 4. Both 33 and 58 KHz BP have typical Q of 8. The outputs of the comparators control separate counters. The ANDed boolean combination of 33 and 58 KHz BP comparator outputs controls a 4th counter as shown in FIG. 3. All comparator outputs are synchronized on the switched-cap clock (1 MHz) and are stable during each period of 1 μs. The counters can be reset or disable by software. An anti-aliasing filter is placed in the first stage. The cut-off frequency is typically 150 KHz. The sampling clock frequency of bandpass filters is F_{1MHz}. Clamping anti-parallel diodes are placed between AREF and DIDT pins internal to the ASIC.

The Z-domain function of the switched-cap bandpass filters can be described by the following expression:

$$Y_i = a (X_i - X_{i-1}) - b Y_{i-1} - c Y_{i-2}$$

Where X_i and Y_i are, respectively, the ith samples of input and output voltages and a, b and c are the filter coefficients.

Coefficient of normalized BP	20 KHz	33 KHz	58 KHz
a	0.031	0.026	0.047
b	-1.953	-1.932	-1.825
c	0.969	0.974	0.952

The output of a ground fault sensing transformer 35 (FIG. 1b) is connected to the input of a GFIN amplifier 80 (FIG. 2), which has a high gain to amplify the small output from the sensor. The ground fault signal is amplified and lowpass filtered (82) (FIG. 2) for anti-aliasing before being fed to the third channel of the multiplexer 32 (FIG. 2).

Referring also to FIG. 4, this circuit performs an amplification and anti-aliasing low pass (LP) filtering of the ground fault (GF) input voltage before A-toD conversion and provides high pass (HP) filtering and amplification for the grounded neutral detection at pin GFOSC. The first gain stage 80 is a current-to-voltage converter providing signal for both low and high pass filters 82, 83 (FIG. 2). The 3 dB bandwidth of the high pass filter will be typical 15 KHz. The LP and HP filters are made by internal resistors and external capacitors 81 and 85 respectively. Clamping anti-parallel diodes 87 (see FIG. 1b) are placed between AREF and GFIN pins for transient protection.

The chip 10 has provision for personnel level ground fault protection when provided with a 5 mA grounded neutral sensing transformer 83 (FIG. 4) as well as the ground fault transformer 35 (FIG. 4). To make this feature functional, the output GFOUT may be coupled by means of a capacitor 81 to the input of GFHF. GFOSC is then capacitively coupled to the winding of the neutral sensing transformer 83. When thus connected, this forms a dormant oscillator neutral detection system, including second opamp 84 and comparator 89. The function of the second amplifier 84 at GFHF is to provide the total loop gain necessary to put the dormant oscillator into oscillation when a sufficiently low resistance grounded neutral condition exists.

The multiplexer 32 (FIG. 2) alternately selects between the three channel inputs, i.e., current, line voltage or ground fault and passes the selected signal to the input of an analog to digital (A/D) converter (ADC) 86 (FIG. 2). The analog to digital converter 86 is a single channel sigma delta converter which alternately digitizes the current, line voltage and ground fault signals for analysis by the microprocessor.

The line current signal at ASIC pin INTEG is obtained by an external low-pass filter 83 placed in the output of the di/dt coil 25 (FIG. 1a). The ASIC amplifies the INTEG signal. An anti-aliasing LP filter is obtained by an external capacitor 88 (FIG. 1b) placed at ICAP pin before A-to-D conversion stage.

The watchdog (WD) 92 monitors the operation of the ARM microprocessor 14. If the software does not reset the watchdog counter at periodic times, the watchdog generates a hard reset of the microprocessor. Alternately, it could be used to cause a trip condition. The watchdog is based on a 15 bit wide periodic counter which is driven by the 250 KHz clock. The counter is reset by software with the WDG_RST address. Writing a 1 on this address resets the counter. As noted, the watchdog must be reset only in a specific time window, otherwise a hard reset is generated. If the watchdog is reset before the counter reaches 2^14 or if the counter is not reset before the counter reaches 2^15, the watchdog reset is generated for the ARM and for the WD counter.

To allow the ARM to check the watchdog value, the MSB (bit 14) can be read and if the value is 1, the processor must reset the counter.

When the watchdog generates a reset, a specific register is set to indicate that a watchdog reset has occurred. This register value can be read even after the reset.

When a trip decision is reached, a trip signal buffer 96 latches and drives the gate of an SCR 98 of an external firing circuit (FIG. 1a). In order to conserve stored energy during the trip sequence, the microprocessor is halted and portions of the analog circuitry are disabled. The SCR 98 is connected in series with a trip coil 100. In the ON state, the SCR 98 causes the coil 100 to be momentarily shorted across the line to mechanically de-latch the contacts of the host device and to subsequently interrupt flow of current.

The push to test (PTT) circuit 102 monitors the status of a push to test (PTT) button 104. When the push to test button is depressed, line voltage is applied through an external voltage divider in circuit 102 to the PTT input of the chip 10. The circuit senses that a system test is being requested and signals the microprocessor to enter a test mode. The activation of the test button 104 (not part of the ASIC) is detected by the PTT comparator 93 (FIG. 2) as a voltage at a PTT (Push-to-Test) pin.

With the microprocessor in the test mode, test signal buffer 106 acts as a current source driving a test winding 45 (FIG. 1a) of the di/dt sensor with a sharply rising and

falling edge square wave at each of the center frequencies of the bandpass filters, namely 20 KHz (when used), 33 KHz and 58 KHz in turn.

TABLE 1 below briefly describes each pin of the ASIC 10.

Name	Type	Description
VSUP	Power	High positive ASIC supply voltage
VDDA	Power	Analog positive ASIC supply voltage and regulator output
VDD	Power	Digital positive ASIC supply voltage (input)
AGND	Power	Analog ground
GND	Power	Digital ground
INTEG	Analog	Input for Current measurement
ICAP	Analog	Input for LP filter
REFIN	Analog	Input sense of reference voltage
AREF	Analog	Analog reference output
DIDT	Analog	Input for DIDT measurement
TEST	Analog	Test output signal
TRIP	Analog	Trip output signal
VL	Analog	Input for voltage measurement
VN	Analog	Input for voltage measurement
VCAP	Analog	Input for LP filter
PTT	Analog	PTT Input signal
CLKI	Analog	Input clock of quartz
CLKO	Analog	Output clock of quartz
GFIN	Analog	Input signal for GF measurement
GFOUT	Analog	Output of gain stage
GFLF	Analog	Input for LP filter
GFHF	Analog	Input for HP filter
GFOSC	Analog	Output of GF dormant gain stage
TDI	Digital - in	Data in
TDO	Digital-out	Data out
TCLK	Digital - in	Clock in
TMS	Digital - in	Select in

TRST Digital - in Reset in (active low)

Additional Operational Description

The ground fault detection feature's primary purpose is to detect arcing to ground, in the incipient stages of arcing, where a grounding conductor is in the proximity of the faulty line conductor. Such detection and tripping can clear arc faults before they develop into major events. As discussed earlier, by the use of appropriate ground fault and neutral sensing transformers, this feature can be used to provide personnel protection as well as arc to ground detection.

When the pust to test button 104 is depressed, line voltage is applied to push to test circuit 102 in such a way as to cause ground fault current to flow through the ground fault sensing transformer 83 and simultaneously force the microcontroller 14 into the test mode as described previously. The microprocessor monitors the output of both the ground fault detection circuitry and the output of the bandpass filters (caused by the test buffer driving the test winding) to determine if the bandpass filter detection circuitry is functional. Only if counters 66 and 68 have sufficiently high counts and sufficiently high ground fault signal peaks are present, will a trip signal be given.

A calibration routine allows the microprocessor 14 to compensate for the offset voltages generated by each of the operational amplifiers in the line voltage, current and ground fault measurement circuits. Immediately following power up and at periodic intervals (to update the data, e.g., to compensate for thermal drift), the microprocessor initiates a calibration procedure. During this time period, the line voltage and current measurement circuits are internally disconnected from their respective input terminals and each of the operational amplifiers is connected in turn to analog reference voltage (AREF) 24. The respective offset voltages (one for each op amp) are then read by the microprocessor and their values are stored in memory. The stored offset voltages are subtracted from the measured signal values by the software. The ground fault offset is measured by internally shorting the first stage amplifier (80) gain setting resistors and reading the offset voltage on an external AC coupling capacitor directly from the input. The software subtracts this value from the measured signal value.

Residential type circuit breakers incorporating arc fault circuit protection require a very small printed wiring board with low power dissipation. Arc fault circuit interruption

requires significant analog and digital signal processing in order to reliably distinguish between arc faults and electrically noisy loads, such as arcs from light switches and universal motors. In a previous embodiment, such processing was achieved using a separate analog ASIC (application specific integrated circuit) and a microcontroller.

The system on chip design provides a reduced package size, approximately 1/3 reduction, as well as a reduction in external components required. The combination of reduced parts and part placement results in a significant cost reduction and ease of assembly. Bandpass filter performance is more consistent, offset voltage correction is improved, test circuit performance is improved, and ground fault personnel protection can be provided.

While particular embodiments and applications of the present invention have been illustrated and described, it is to be understood that the invention is not limited to the precise construction and compositions disclosed herein and that various modifications, changes, and variations may be apparent from the foregoing descriptions without departing from the spirit and scope of the invention as defined in the appended claims.